Scaling carbon nanotube complementary transistors to the 5 nm gate length and toward the quantum limit

Subject Code: F01

With the support by the National Natural Science Foundation of China, the research team led by Prof. Peng Lianmao (**彭练矛**) and Prof. Zhang Zhiyong (**张志勇**) at the Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing, recently reported that carbon nanotube CMOS FETs were scaled down to the 5 nm gate length and presented performance nearly to the quantum limit, in *Science* (2017, 355: 271—276).

High-performance carbon nanotube field-effect transistors (CNT FETs) with a gate length of 5 nm have been fabricated that perform better than silicon CMOS FETs at the same scale. A scaling trend study revealed that the scaled CNT-based devices, which use graphene contacts, can operate much faster and at much lower supply voltage (0.4 versus 0.7 volts) and with a much smaller subthreshold slope (typically 73 millivolts per decade). The 5-nm CNT FETs approached the quantum limit of FETs by using only one electron per switching operation. In addition, the contact length of the CNT CMOS devices was scaled down to 25 nm, and a CMOS inverter with a total pitch size of 240 nm was demonstrated. These results show that CNT CMOS technology has the potential to substantially outperform Si when approaching the quantum limits of a binary logic switch and to extend mainstream CMOS technology in the post-Moore era.

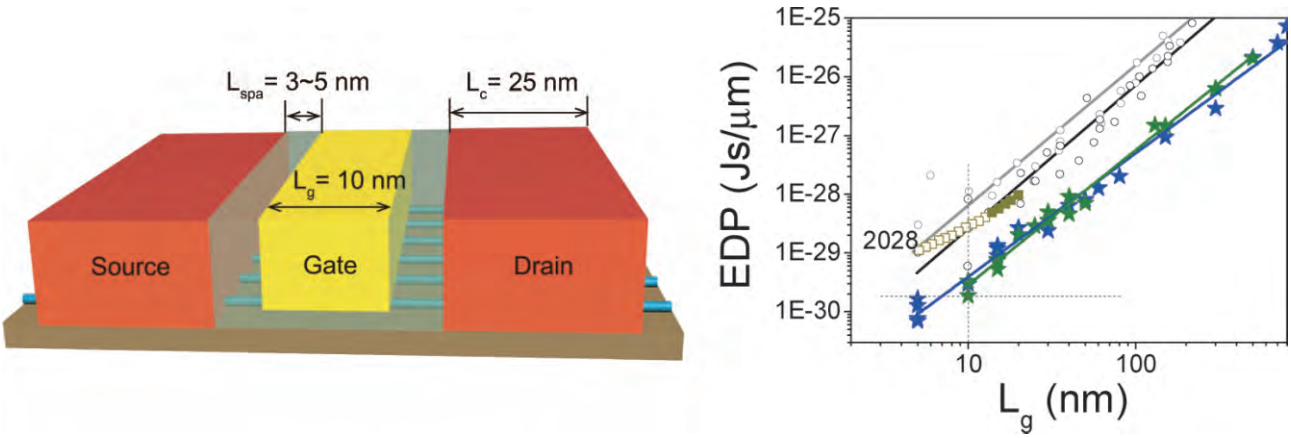

Figure Schematic diagram (left) and performance (right) of CNT CMOS FETs, showing that CNT CMOS FETs (stars) are 10 times better than Si CMOS (circles) on speed and power dissipation comprehensively (in terms of EDP: energy delay product).